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10/690,946	10/22/2003	John D. Anderson	A-8764	6186

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EXAMINER	
CAVALLARI, DANIEL J	

ART UNIT	PAPER NUMBER
2836	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTOmail@sciatl.com

Office Action Summary	Application No.	Applicant(s)	
	10/690,946	ANDERSON ET AL.	
	Examiner	Art Unit	
	Daniel Cavallari	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,18,21 and 23-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21 and 27-30* is/are allowed.

6)☒ Claim(s) *1-11,18,23-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments, see Remarks, Page 11, filed 11/8/2007, with respect to the claim objections of 1-8 have been fully considered and are persuasive. The claim objection of claims 1-8 has been withdrawn.

The Examiner notes that it was explained that an "inverting switch" is not a term ordinarily used in the art. The specification and drawings describe what is meant by the applicant's "inverting switch" however the recitation of an "inverting switch" in the claim 1 does not provide any physical limitations of the "inverting switch" and the term is a combination of two known terms "inverter" and "switch" however it's combination into a single term is not known. The Examiner pointes out in the rejection because no physical limitations were provided for the "inverting switch" and because it is unclear what is meant by this term which is a combination of two components not ordinarily combined, the term "inverting switch" would be examined as "any device capable of performing any form of electrical inversion and is not limited to either a conventional switch nor a conventional inverter" and since no objection was made to this interpretation, the interpretation will be taken as correct.

Applicant's arguments in regard to the 112 second paragraph rejection of claims 1 & 18 have been fully considered but they are not persuasive.

The applicant argues that the relative terms "substantially-immediate" and "substantially-instantaneous" are not improper and sites case law which points out that "such terms should be interpreted in light of the specification to determined the literal coverage of the claim" (*Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988), cert. denied, 488 U.S. 825 (1988)*) and "words of degree in the claims were not indefinite because the specification provided an indication as to how to measure that degree" (*Seattle Box Co., Inc. v. Industrial Crating & Packaging, Inc., 756 F.2d 1574 (Fed. Cir. 1985)*).

The applicant goes on to point to the specification that allegedly teaches the terms "substantially-immediate" and "substantially-instantaneous".

> When the inverting switch 106 is in operation, the value of the voltage at the connection 401 determines whether the transistors Q.sub.1 and Q.sub.2 are on (i.e., conducting between their respective collectors and emitters). The transistors Q.sub.1 and Q.sub.2 are turned on when the voltage at the connection 401 is "high", and vice versa. When the transistors Q.sub.1 and Q.sub.2 are on, the voltage V.sub.5 is "low," and vice versa. The capacitor C2 causes a small delay (for example, among others, 30 milliseconds) between the time that the voltage at the connection 401 transitions from "low" to "high" and the time that the transistor Q.sub.2 turns on. A "high" to "low" transition at connection 401 immediately turns off transistor Q.sub.1 which causes the voltage V.sub.5 to transition "high" regardless of the turn off delay of transistor Q.sub.2. This "Instant on--delayed off" switching allows for a more constant voltage output of the power-switching circuit 100 by completely draining the old supply while the new supply is being loaded.

The Examiner notes that the only mention of any particular time in the specification is "for example, among others, 30 milliseconds" which fails to provide any mention of this equating to either "substantially-immediate" and "substantially-instantaneous". The specification lacks any recitation of the terms "substantially-

immediate" and "substantially-instantaneous" and therefore fails to provide a literal coverage of the term or an indication as to how to measure either of the terms degree.

Applicant's arguments in regard to the 102 rejection of claims 1, 2, 3, 5, & 6 by Eitan have been fully considered but they are not persuasive.

Applicant argues that Eitan fails to disclose an inverting switch comprising a delay circuit and makes the argument "Even assuming arguendo the right most inverter 48 can be equated to the inverter switch in claim 1 and the left most inverter can be equated to a delay circuit, it cannot be properly said that the right most inverting switch 48 "comprises" the left most inverter. The Examiner respectfully disagrees. The "inverting switch" comprises **both** inverters 48. The Examiner points out that the left most inverter was designated as the "delay circuit" portion of the "inverting switch" of both inverters 48 (also shown as 46). This is provided in the previous rejection of claim 1 "...the inverting switch further comprising a delay circuit (read on by the left most inverter, 48, See Figure 2)" which discloses both the delay circuit AND that the "inverting switch" is taken to **comprise** this left most inverter.

Applicant's arguments in regard to the 102 rejection of claims 1 & 6-11 by Little have been fully considered but they are not persuasive.

The applicant argues "Little fails to disclose, teach, or suggest at least the above-emphasized claim features, and hence respectfully request that the rejection be withdrawn". Those emphasized claim features in question will be taken as the bolded text "the inverting switch further comprising a delay circuit".

The Examiner respectfully disagrees and points out that the delay circuit is provided by the inverters (such as 60, 62) as explained in the rejection of claim 1 "The examiner notes that an inverter inverts the input (from inverter 62) and provides it to the output (gate of transistor 18)..." More specifically, inverter 60 (Figure 1A) provides this delay. Therefore, "inverter switch" does in fact comprise a delay circuit wherein the "inverter switch" comprises components 63 and 60.

Claim Objections

Claim 18 is objected to because of the following informalities:

Claim 18 recites "the delayed-off output of a longer duration that substantially instantaneous..." which is grammatically incorrect.

Furthermore, the "delayed-off output duration" is unclear as it is the delayed-off output transition duration which is being referenced and not the duration of the output signal itself (as in how long the output is held high but rather how long it takes to switch from a high to low signal once the switch is signaled to be switched), as the claim language suggests.

The claim language should clearly state that it is the transition times of the outputs being referred to and the claim should be corrected and checked for grammatical errors.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

The term ""substantially-immediate" and "substantially instantaneous" in claims 1 & 18 are relative terms which renders the claim indefinite. The term "substantially" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

The claim will be examined as best understood.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 & 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Eitan et al. (US 5,886,561).

Eitan et al. teaches:

In regard to Claims 1

- A threshold detector circuit, read on by comparator (20).
- A first switching circuit (24) for enabling access to a back-up power source (14), the first switching circuit comprising at least one transistor (24) (See figure 1).
- An inverting switch (read on by the right most inverter, 48, See Figure 2) coupled between the first switching circuit (24) and the threshold detector circuit (20), the inverting switch comprising an input and an output, the inverting switch configured to receive a signal at the input, invert the signal, and provide the inverted signal from the output to the first switching circuit (24), the inverting switch further comprising a delay circuit (read on by the left most inverter, 48, See Figure 2) configured to provide a substantially-immediate high output during an off-to-on transition at the output of the inverting switch [The Examiner notes the transistor (24, Figure 1) transitions from off-to-on by being provided a low voltage therefore the input of the right inverter (48) (See Figure 2) must be high] and a switching delay during on-to-off transition at the output of the inverting switch [The examiner notes the inverter (48) provides a delay].
- Wherein the threshold detector circuit (20) is configured to cause the first switching circuit (24) to enable access to the back-up power source (14) responsive to the voltage provided by a primary power source dropping below a predetermined threshold (See Column 3, Lines 1-15).

(See Figure 1)

In regard to Claim 2

- A second switching circuit, read on by transistor switch (26) enabling access to a primary source.

In regard to Claim 3

- The threshold detector (20) is configured to cause the first switching circuit to enable or terminate access to the main power source responsive to the voltage provided by a primary power source rising above a predetermined threshold (See Column 3, Lines 35-63 & Column 1, Line 62 to Column 2, Line 11).

In regard to Claim 5

- Wherein the inverting switch (48) comprises at least one transistor [The examiner notes that Eitan discloses an inverter (53) comprising transistors (See Figure 4)].

In regard to Claim 6

- An inverter (left most inverter, 48, Figure 2) coupled between the inverting switch (right most inverter, 48, Figure 2) and the threshold detector circuit (40, 42, 44, Figure 2).

Claims 1, & 6-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Little et al. (US 4,908,790).

In regard to Claim 1

- A threshold detector circuit, read on by comparator (32).
- A first switching circuit (14) for enabling access to a back-up power source (19), the first switching circuit comprising at least a first transistor (14).
- An inverting switch (63) coupled between the first switching circuit (14) and the threshold detector circuit (32), the inverting switch comprising an input and an output, the inverting switch configured to receive a signal at the input, invert the signal, and provide the inverted signal at the output to the first switching circuit (14), the inverting switch further comprising a delay circuit (60) configured to provide a substantially-immediate high-output during an off-to-on transition at the output of the inverting switch switching delay during an on-to-off transition at the output.
- Wherein the threshold detector circuit (32) is configured to cause the first switching circuit (14) to enable access to the back-up power source (19) responsive to the voltage provided by a primary power source (11) dropping below a predetermined threshold (See Column 5, Lines 41-62 & Column 7, Line 55 to Column 8, Line 5).

[The examiner notes that the first switch (14) enables access to the back-up power supply by disconnecting power to a primary power supply (11)].

In regard to Claim 6

- An inverter (62, 34) coupled between the inverting switch (60, 63) and the threshold detector circuit (32) (See figure 1).

In regard to Claim 7

- The inverter (62, 34) further comprising a comparator (34) (See Figure 1).

In regard to Claim 8

- A second transistor (18) coupled to the first transistor (14) (See Figure 1).

In regard to Claim 9

- The emitter of the first transistor is coupled to the collector of the second transistor (See Figure 1).

In regard to Claim 10

- Wherein current flow between the first and second transistor terminates access to the back-up power source [The examiner notes that current flow between the first (18) and second (14) transistors (between the primary source 11 and load 17) terminates access to the back-up power source when the voltage is above the predetermined value thus supply power (and current) to the load and between the switches (See figure 1)].

In regard to Claim 11

- Wherein resistance to current flow between the first and second transistors enables access to the back-up power source [The examiner notes that resistance between the switches (14 & 18) is read on by the switches being open which enables access ot the back-up power source (19) (See figure 1)].

Allowable Subject Matter

Claims 21 & 27-30 are allowed for reasons indicated in the previous office action dated 7/28/2006.

Claim 18 would be allowable if re-written to overcome the 112 second paragraph rejection disclosed at the beginning of this office action. Reasons for allowance are stated below.

Claims 23, 24, 25, & 26 are rejected because of the 112 second paragraph rejection of independent claim 18 but would be allowable if claim 18 is re-written to overcome the 112 second paragraph rejection.

In regard to Claim 18

Claim 18 includes a system comprising an inverting switch wherein the delayed-off output of the switch is of a longer duration than the substantially instantaneous transition of the high output during an on-to-off transition.

Davis et al. (US 5,191,229) teaches the inverting switch (See Dais et al. Figure 1, components 30, 60, 50, & 32 wherein the delayed-off output of the switch is of a longer duration than the substantially instantaneous transition of the high output during an on-to-off transition however there is a lack of motivation to combine this switch structure with the system of Eitan et al. (US 5,886,561).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel Cavallari whose telephone number is 571-272-8541. The examiner can normally be reached on Monday-Friday 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571)272-2800 x36. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

1/17/08

Daniel Cavallari

January 14, 2008